

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

 ATTY. DOCKET NO.
43876-145

 SERIAL NO.
10/646,787

 APPLICANT
HANSEN, et al.

 FILING DATE
August 25, 2003

GROUP

(PTO-1449)

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
AS	4,025,772	05/24/77	Constant			
	4,489,393	12/18/84	Kawahara, et al.			
	4,701,875	10/20/87	Konishi, et al.			
	4,727,505	02/23/88	Konishi, et al.			
	4,876,660	10/24/89	Owens, et al.			
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	4,956,801	09/11/90	Priem et al.			
	4,969,118	11/06/90	Montoye, et al.			
	4,975,868	12/04/90	Freerksen			
	5,032,865	07/16/91	Schlunt			
	5,157,388	10/20/92	Kohn			
	5,201,056	04/06/93	Daniel, et al.			
	5,268,855	12/07/93	Mason, et al.			
AS	5,268,995	12/07/93	Diefendorff, et al.			

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EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						Yes	No

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AS	Parallel Computers for Graphics Applications, Adam Levinthal, Pat Hanrahan, Mike Paquette, Jim Lawson, Pixar San Rafael, California, 1987
	Organization of the Motorola 88110 Superscalar RISC Microprocessor, Keith Diefendorff and Michael Allen.
AS	Microprocessor Report, Volume 7 Number 13, October 4, 1993, IBM Regains Performance Lead with Power2, Six Way Superscalar CPU in MCM Achieves 126 SPECint92.
	IBM Creates PowerPC Processors for AS/400, Two New CPU's Implement 64-Bit Power PC with Extensions by Linley Gwennap, July 31, 1995.

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4/14/05

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INFORMATION DISCLOSURE CITATION IN AN APPLICATION

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U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
<i>AS</i>	5,408,581	04/18/95	Suzuki, et al.			
	5,423,051	06/06/95	Fuller, et al.			
	5,426,600	06/20/95	Nakagawa, et al.			
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	5,557,724	09/17/96	Sampat, et al.			
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	5,592,405	01/07/97	Gove, et al.			
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	5,642,306	06/24/97	Mennemeier, et al.			
	5,666,298	09/09/97	Peleg, et al.			
	5,669,010	09/16/97	Duluk, Jr.			
	5,673,407	09/30/97	Poland, et al.			
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						Yes	No
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	0 654 733 A1	05/07/94	Germany				

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<i>AS</i>	The Visual Instruction Set (VIS) in UltraSPAR™, L. Kohn, G. Maturana, M. Tremblay, A. Prabhu, G. Zyner, May 3, 1995.
	Osborne McGraw-Hill, i860™ Microprocessor Architecture, Neal Margulis, Foreword by Les Kohn
<i>AS</i>	A General-Purpose Array Processor for Seismic Processing, Nov-Dec., 1984, Volume 1, No. 3). Revisiting past digital signal processor technology, Don Shaver- Jan-Mar. 1998.
<i>AS</i>	Accelerating Multimedia with Enhanced Microprocessors, Ruby B. Lee, 1995.

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<i>[Signature]</i>	5,721,892	02/24/98	Peleg, et al.			
	5,734,874	03/31/98	Van Hook, et al.			
	5,757,432	05/26/98	Dulong, et al.			
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	5,922,066	07/13/99	Cho, et al.			
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	6,092,094	07/18/00	Ireton			
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EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
A		US 4,785,393	11/15/1988	Chu et al.	
		US 4,814,976	03/21/1989	Craig C. Hansen, et al.	
		US 5,031,135	07/09/1991	Patel	
		US 5,280,598	01/1994	Osaki et al.	
		US 5,481,686	01/02/1996	Dockser	
		US 5,487,024	01/1996	Girardeau Jr.	
		US 5,600,814	02/1997	Gahan et al.	
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		US 5,742,840	04/21/1998	Hansen et al.	
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B		6,275,834 B1	08/14/2001	Derrick Chu Lin, et al.	
		6,295,599	09/2001	Hansen et al.	

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EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Codes-Number + -Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation	
						Yes	No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
A		IEEE Draft Standard for "Scalable Coherent Interface-Low-Voltage Differential Signal Specifications And Packet Encoding", IEEE Standards Department, P1596.3/D0.15 (March 1992)
		IEEE Draft Standard for "High-Bandwidth Memory Interface Based on SCI Signaling Technology (RamLink)", IEEE Standards Department, Draft 1.25 IEEE P1596.4-199X (May 1995)
		IBM, "The PowerPC Architecture: A Specification For A New Family of Risc Processors", 2nd Ed., Morgan Kaufmann Publishers, Inc., (1994).
B		Hewlett-Packard Co., "PA-RISC 1.1 Architecture and Instruction Set", Manual Part No. 09740-90039, (1990).
		MIPS Computer Systems, Inc., "MIPS R4000 User's Manual", Mfg. Part No. M8-00040, (1990).

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¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.